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PATENT  
Attorney Docket No. ASC-025DV1C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Cheng *et al.*  
SERIAL NO.: 10/802,185 GROUP NO.: 2813  
FILING DATE: March 17, 2004 EXAMINER: Craig Thompson  
TITLE: SEMICONDUCTOR SUBSTRATE STRUCTURE

**CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8**

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 8<sup>th</sup> day of April, 2005.

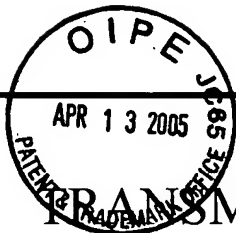
  
Wendy L. Martin

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith are:

1. Transmittal Form (1 page);
2. Supplemental Information Disclosure Statement (1 page);
3. Form PTO – 1449 (4 pages);
4. Copies of cited references (C144 – C164); and
5. Return receipt postcard



# TRANSMITTAL FORM

Application Serial Number	10/802,185
Filing Date	March 17, 2004
First Named Inventor	Cheng
Group Art Unit	2813
Examiner Name	Craig Thompson
Attorney Docket No.	ASC-025DV1C1

## ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Check Attached <input type="checkbox"/> Copy of Fee Transmittal Form	<input type="checkbox"/> Copy of Notice to File Missing Parts of Application	<input type="checkbox"/> Notice of Appeal to Board of Patent Appeals and Interferences
<input type="checkbox"/> Amendment/Response <input type="checkbox"/> Preliminary <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Letter to Official Draftsperson including Drawings [Total Sheets ____]	<input type="checkbox"/> Formal Drawing(s)	<input type="checkbox"/> Appeal Brief (in triplicate)
<input type="checkbox"/> Petition for Extension of Time	<input type="checkbox"/> Request For Continued Examination (RCE) Transmittal	<input type="checkbox"/> Status Inquiry
<input checked="" type="checkbox"/> Supplemental Information Disclosure Statement <input checked="" type="checkbox"/> Form PTO-1449 <input checked="" type="checkbox"/> Copies of IDS Citations (C144 - C164)	<input type="checkbox"/> Power of Attorney (Revocation of Prior Powers)	<input checked="" type="checkbox"/> Return Receipt Postcard
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> Terminal Disclaimer	<input checked="" type="checkbox"/> Certificate of First Class Mailing under 37 C.F.R. 1.8
<input type="checkbox"/> Sequence Listing submission <input type="checkbox"/> Paper Copy/CD <input type="checkbox"/> Computer Readable Copy <input type="checkbox"/> Statement verifying identity of above	<input type="checkbox"/> Executed Declaration and Power of Attorney for Utility or Design Patent Application	<input type="checkbox"/> Certificate of Facsimile Transmission under 37 C.F.R. 1.8
	<input type="checkbox"/> Small Entity Statement	<input type="checkbox"/> Additional Enclosure(s) (please identify below)
	<input type="checkbox"/> CD(s) for large table or computer program	
	<input type="checkbox"/> Amendment After Allowance	
	<input type="checkbox"/> Request for Certificate of Correction <input type="checkbox"/> Certificate of Correction (in duplicate)	

## CORRESPONDENCE ADDRESS

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## SIGNATURE BLOCK

Respectfully submitted,  
  
Date: April 8, 2005  
Reg. No. 44,381  
Tel. No.: (617) 570-1806  
Fax No.: (617) 523-1231  
  
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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Sir:

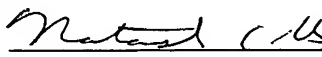
The references listed on the enclosed PTO-1449 and enclosed herewith are submitted solely in compliance with the duty of candor. It is understood that this Information Disclosure Statement does not fall within the provisions of 37 C.F.R. §1.97.

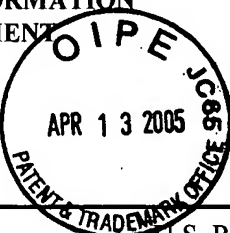
It is respectfully requested that the publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application. In accordance with the U.S. Patent Office's partial waiver of the requirement under 37 C.F.R. 1.98(a)(2)(i), only copies of the non-patent publications are enclosed.

Respectfully submitted,

Date: April 8, 2005  
Reg. No. 44,381

Tel. No.: (617) 570-1806  
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<b>FORM PTO – 1449</b>  <b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>				<b>ATTORNEY DOCKET NO.:</b> ASC-025DV1C1  <b>APPLICANT(S):</b> Cheng <i>et al.</i>  <b>SERIAL NO.:</b> 10/802,185  <b>FILING DATE:</b> March 17, 2004  <b>GROUP:</b> 2813			
							
<b>U.S. PATENT DOCUMENTS</b>							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
		A255	2002/0063292	05/30/2002	Armstrong <i>et al.</i>		
		A256	2002/0190284	12/19/2002	Murthy <i>et al.</i>		
		A257	2004/0007724	01/15/2004	Murthy <i>et al.</i>		
		A258	2004/0014276	01/22/2004	Murthy <i>et al.</i>		
		A259	2004/0070035	04/15/2004	Murthy <i>et al.</i>		
		A260	2004/0084735	05/06/2004	Murthy <i>et al.</i>		
		A261	2004/0119101	06/24/2004	Schrom <i>et al.</i>		
		A262	2004/0142545	07/22/2004	Ngo <i>et al.</i>		
		A263	2004/0173815	09/09/2004	Yeo <i>et al.</i>		
		A264	5,089,872	02/18/1992	Ozturk <i>et al.</i>		
		A265	5,242,847	09/07/1993	Ozturk <i>et al.</i>		
		A266	6,228,694	05/08/2001	Doyle <i>et al.</i>		
		A267	6,235,568	05/22/2001	Murthy <i>et al.</i>		
		A268	6,281,532	08/28/2001	Doyle <i>et al.</i>		
		A269	6,326,664	12/04/2001	Chau <i>et al.</i>		
		A270	6,563,152	05/13/2003	Roberds <i>et al.</i>		
		A271	6,605,498	08/12/2003	Murthy <i>et al.</i>		
		A272	6,621,131	09/16/2003	Murthy <i>et al.</i>		
		A273	6,657,223	12/02/2003	Wang <i>et al.</i>		
		A274	6,703,648	03/09/2004	Xiang <i>et al.</i>		
		A275	6,743,684	06/01/2004	Liu		
<b>EXAMINER</b>				<b>DATE CONSIDERED</b>			

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<b>FOREIGN PATENT DOCUMENTS</b>									
<b>EXAM. INIT.</b>		<b>DOCUMENT NUMBER</b>	<b>DATE</b>	<b>COUNTRY CODE</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE</b>	<b>ABSTRACT ONLY</b>	<b>ENGLISH LANG (Y/N)</b>
<b>OTHER ART, JOURNAL ARTICLES, ETC.</b>									
<b>EXAM. INIT.</b>	<b>OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)</b>								
	C144	Gannavaram, <i>et al.</i> , "Low Temperature ( $\leq 800^{\circ}\text{C}$ ) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> , (2000), pp. 437-440.							
	C145	Ge <i>et al.</i> , "Process-Strained Si (PSS) CMOS Technology Featuring 3D Strain Engineering," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2003) pp. 73-76.							
	C146	Ghani <i>et al.</i> , "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2003), 978-980.							
	C147	Hamada <i>et al.</i> , "A New Aspect of Mechanical Stress Effects in Scaled MOS Devices," <u>IEEE Transactions on Electron Devices</u> , Vol. 38, No. 4 (April 1991), pp. 895-900.							
	C148	Huang <i>et al.</i> , "Isolation Process Dependence of Channel Mobility in Thin-Film SOI Devices," <u>IEEE Electron Device Letters</u> , Vol. 17, No. 6 (June 1996), pp. 291-293.							
	C149	Huang <i>et al.</i> , "LOCOS-Induced Stress Effects on Thin-Film SOI Devices," <u>IEEE Transactions on Electron Devices</u> , Vol. 44, No. 4 (April 1997), pp. 646-650.							
	C150	Huang, <i>et al.</i> , "Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $\text{Si}_{1-x}\text{Ge}_x$ Source/Drain", <u>IEEE Electron Device Letters</u> , Vol. 21, No. 9, (Sept. 2000) pp. 448-450.							
	C151	Iida <i>et al.</i> , "Thermal behavior of residual strain in silicon-on-insulator bonded wafer and effects on electron mobility," <u>Solid-State Electronics</u> , Vol. 43 (1999), pp. 1117-1120.							
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				

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OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C152	Ito <i>et al.</i> , "Mechanical Stress Effect on Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2000), pp. 247-250.							
	C153	Lochtefeld <i>et al.</i> , "Investigating the Relationship Between Electron Mobility and Velocity in Deeply Scaled NMOS via Mechanical Stress," <u>IEEE Electron Device Letters</u> , Vol. 22, No. 12 (2001), pp. 591-593.							
	C154	Ootsuka <i>et al.</i> , "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Applications," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2000), pp. 575-578.							
	C155	Ota <i>et al.</i> , "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2002), pp. 27-30.							
	C156	Öztürk, <i>et al.</i> , "Advanced Si <sub>1-x</sub> Ge <sub>x</sub> Source/Drain and Contact Technologies for Sub-70 nm CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> , (2002), pp. 375-378.							
	C157	Öztürk, <i>et al.</i> , "Low Resistivity Nickel Germanosilicide Contacts to Ultra-Shallow Si <sub>1-x</sub> Ge <sub>x</sub> Source/Drain Junctions for Nanoscale CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> (2003), pp. 497-500.							
	C158	Öztürk, <i>et al.</i> , "Selective Silicon-Germanium Source/Drain Technology for Nanoscale CMOS," <u>Mat. Res. Soc. Symp. Proc.</u> , Vol. 717, (2002), pp. C4.1.1-C4.1.12.							
	C159	Öztürk, <i>et al.</i> , "Ultra-Shallow Source/Drain Junctions for Nanoscale CMOS Using Selective Silicon-Germanium Technology," <u>Extended Abstracts of International Workshop on Junction Technology</u> , (2001), pp. 77-82.							
EXAMINER					DATE CONSIDERED				

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	C160	Shimizu <i>et al.</i> , "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2001), pp. 433-436.							
	C161	Thompson <i>et al.</i> , "A Logic Nanotechnology Featuring Strained-Silicon," <u>IEEE Electron Device Letters</u> , Vol. 25, No. 4 (April 2004), pp. 191-193.							
	C162	Thompson <i>et al.</i> , "A 90 nm Logic Technology Featuring 50nm Strained-Silicon Channel Transistors, 7 layers of Cu <i>Interconnects</i> , Low k ILD, and 1um <sup>2</sup> SRAM Cell," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2002), pp. 61-64.							
	C163	Tiwari <i>et al.</i> , "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (1997), pp. 939-941.							
	C164	Uchino, <i>et al.</i> , "A Raised Source/Drain Technology Using In-situ P-doped SiGe and B-doped Si for 0.1-μm CMOS ULSIs," <u>IEEE International Electron Device Meeting Technical Digest</u> , (1997), pp. 479-482.							
EXAMINER					DATE CONSIDERED				